Abstract

A content addressable memory (CAM) architecture. For one embodiment, the CAM architecture includes a plurality of rows of CAM cells, each row configured to generate match results on a corresponding match line, a number of comparand lines, each coupled to a corresponding CAM cell in each of the plurality of rows of CAM cells, a plurality of timed storage circuits, each having a data input coupled to a corresponding match line and having an enable input coupled to an enable signal line, a timing generator configured to generate an enable signal on the enable signal line, and a plurality of load elements.